NEWT Microprocessor

(Nut, Extended, With Turbo)

and

41CL Calculator

Monte Dalrymple

Why?

Demonstrate moving a design to a new technology

Higher performance

Internal modules

Exercise design skills

The “Nut” Part

CPU used in 11C, 12C, 15C, 16C and 41C

Cloned from public documentation

Includes most, but not all, “bugs”

Verilog HDL description only requires 19 pages

The “Extended” Part

Direct interface to standard 16-bit memories

Two Chip Selects (Flash & RAM)

Memory Management Unit for 20-bit physical address

MMU maps 4K pages/banks

Registers & X-memory mapped to RAM

The “With Turbo” Part

18MHz input frequency

Normal divider speed is /50, for 360KHz operation

Programmable speed: 1x, 2x, 5x, 10x, 20x, 50x

Serial bus is always 1x for compatibility

Dynamic execution speed for compatibility

Tagged execution speed for compatibility

The “41CL” Part

NEWT design in a Flash FPGA

512Kx16 and 128Kx16 RAM

Power control & regulation via discretes/SMT

Replace the CPU board in a Fullnut

Current Status

Nut clone complete

NEWT complete except for physical memory interface

What remains

Complete the design

Breadboard replacement CPU board

Build the real hardware

Write the software to use it